What is claimed is: redundancy

1. An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals; and

feedback ~~means~~ circuit interconnecting said memory devices and cross-coupling signals produced by said memory devices.

2. The improved digital-data receiver synchronization apparatus of claim 1, further comprising:

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices.

3. The improved digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals include at least one signal selected from the group consisting of an RF carrier signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, and a data burst- or packet-rate signal.

4. The improved digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are integrally or fractionally related in frequency, phase or both frequency and phase.

5. The improved digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are rationally multiply related in frequency and/or phase.

6. The improved digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals satisfy the relationship

$$f_1 = M \cdot f_2 = M \cdot N \cdot f_3$$

wherein f_1 is said RF signal; f_2 is said data bit rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

7. The improved digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference is an oscillator controlled by a crystal, SAW device, ceramic resonator, mechanical resonator, dielectric resonator, or external source.

8. The improved digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference uses edge- triggered synchronous logic.

9. The improved digital-data receiver synchronization apparatus of claim 2, wherein said signals cross-coupled by said feedback means include at least one signal selected from the group consisting of error signals, output signals, and both error and output signals.

10. The improved digital-data receiver synchronization apparatus of claim 1, wherein said signals cross-coupled by said feedback means are analog signals.

11. The improved digital-data receiver synchronization of claim 1, wherein said signals cross-coupled by said feedback means are digital signals.

12. The improved digital-data receiver synchronization apparatus of claim 1, wherein said memory devices are phase-locked loops.

13. An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector; defined

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback ~~means~~ circuit interconnecting said memory devices and for cross-coupling certain signals produced by said memory devices.

14. The improved digital-data receiver synchronization apparatus of claim 13, wherein said multiple timing signals include at least one of an RF signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, and a data burst- or packet-rate signal.

15. The improved digital-data receiver synchronization apparatus of claim 13, wherein said multiple timing signals satisfy the relationship:

$$f_1 = M \cdot f_2 = M \cdot N \cdot f_3$$

wherein f_1 is said RF signal; f_2 is said data bit-rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

16. The improved digital-data receiver synchronization apparatus of claim 13, wherein said common frequency reference uses edge-triggered synchronous logic.

17. The improved digital-data receiver synchronization apparatus of claim 13, wherein said signals cross-coupled by said feedback means include at least one signal selected from the group consisting of error signals, output signals, and both error and output signals.

18. The improved digital-data receiver synchronization apparatus of claim 13, wherein said composite phase-frequency detector comprises at least one device selected from the group consisting of: a digital phase-frequency detector; a standard analog RF mixer; a standard analog multiplier; a digital XOR gate; a digital J-K flip-flop; a digital trigger (T) flip-flop; a digital R-S flip-flop; and a digital counter;

19. The improved digital-data receiver synchronization apparatus of claim 13, wherein said composite phase-frequency detector further includes at least one device selected from the group consisting of: a switch; a relay; a digital trigger (T) flip-flop; a digital divider; a nonlinear element; an analog divider; a square-root circuit; a comparator; a frequency-to-voltage converter; a frequency-to-current converter; a digital AND gate; a digital OR gate; a digital XOR

gate; a digital counter; a digital J-K flip-flop; a digital R-S flip-flop; a majority-logic circuit; a peak detector; an average detector; a root-mean-square (RMS) detector; an operational amplifier; a follower circuit; a logic array device; a microprocessor; a digital state machine; a neural network; a digital signal processor (DSP) device; and an analog signal processor (ASP) device.

20. The improved digital-data receiver synchronization apparatus of claim 13, wherein said composite phase-frequency detector comprises a timing device for limiting the detector signal pulse widths.

21. The improved digital-data receiver synchronization apparatus of claim 13, wherein said composite phase-frequency detector further comprises at least one device selected from the group consisting of: a monostable multivibrator; a delay generator; a digital counter; a logic gate; a switch; a digital state machine; a pulse width-to-voltage converter; a pulse width-to-current converter; an integrator; a comparator; and a pulse width-limiting circuit.

22. The improved digital-data receiver synchronization apparatus of claim 13, wherein said composite phase-frequency detector further comprises an input-signal rate-limiting amplifier whereby said composite phase-frequency detector will not follow a signal having oscillations above a predetermined rate of change.

23. The improved digital-data receiver synchronization apparatus of claim 22, wherein said rate of change is measured in voltage (volts) per second.

24. The improved digital-data receiver synchronization apparatus of claim 22, wherein said rate of change is measured in current (amps) per second.

25. An improved digital data receiver synchronization apparatus for receiving data signals

from a transmitter, said apparatus comprising:

first synchronization means for synchronizing a first frequency signal with a first received data signal and for generating a first comparison signal;

second synchronization means for synchronizing a second frequency signal with a second received data signal and for generating a second comparison signal;

first interconnection means for transmitting said first comparison signal to said second synchronization means;

second interconnection means for transmitting said second comparison signal to said first synchronization means;

said first synchronization means comprising a first corrective means for adjusting said first frequency signal in response to said second comparison signal; and

said second synchronization means comprising a second corrective means for adjusting said second frequency signal in response to said first comparison signal.

26. The improved digital-data receiver synchronization apparatus according to claim 25, wherein said first frequency signal and said second frequency signal are derived from a common source.

27. The method of providing improved digital-data receiver synchronization comprising the steps of:

providing a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector, each of said plurality of memory devices providing an output comparison signal; and,

interconnecting said memory devices with a feedback means for cross-coupling said output comparison signals produced by said memory devices.

28. The method according to claim 27, further comprising the step of:

connecting a common frequency reference source with said plurality of memory devices for driving said plurality of memory devices.

29. A method of providing improved digital-data receiver synchronization of received data signals comprising the steps of:

providing a first synchronization means for synchronizing a first frequency signal with a first received data signal and for generating a first comparison signal;

providing a second synchronization means for synchronizing a second frequency signal with a second received data signal and for generating a second comparison signal;

transmitting said first comparison signal to said second synchronization means;

transmitting said second comparison signal to said first synchronization means;

adjusting said first frequency signal in response to said second comparison signal; and

adjusting said second frequency signal in response to said first comparison signal.